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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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GARLICK HARRISON & MARKISON LLP			MEEK, JACOB M	
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AUSTIN, TX 78716-0727			PAPER NUMBER	
			2637	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/086,267

Applicant(s)

AGAZZI, OSCAR E.

Examiner

Jacob Meek

Art Unit

2637

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 March 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 184 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 - 184 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 March 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Double Patenting

1. Applicant is advised that should claim 175 be found allowable, claims 176, 179, and 181 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. Applicant is advised that should claim 178 be found allowable, claims 177, 180, and 182 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 –29, 34 – 71, 76 – 79, 113 – 116, 119 - 128, 134 – 162, 167 - 174, 179, and 180 are rejected under 35 U.S.C. 102(e) as being anticipated by Phanse (US-6,795,494).

With regard to claim 1, Phanse discloses a DSP based serializer / de-serializer (see abstract) comprising: a receiver that includes an A/D converter and a DSP, the DSP is operably coupled to the output of the A/D converter (see figure 1, 145, 150, 180 and abstract); wherein A/D converter samples modulated serial data to generate digital samples of modulated serial data (see figure 1, 145 and abstract); and the DSP adaptively determines compensation operations to be performed by the receiver on digital samples of modulated serial data so that digital samples of modulated serial data may be properly characterized to extract digital data contained therein (see abstract).

With regard to claim 2, Phanse discloses DSP SERDES interfaces 2 devices communicatively coupled via at least one of a twisted pair, coax, or twin-ax cable (see column 6, lines 6 – 14 where a 2nd device is required for an operable link).

With regard to claim 3, Phanse discloses existence of 1st and 2nd on-board traces (see column 8, lines 34 – 39 where a 2nd device is required for an operable link).

With regard to claim 4, Phanse discloses existence of 1st and 2nd IC (see figure 1, 101 and column 8, lines 34 – 39 where a 2nd device is required for an operable link).

With regard to claim 5, Phanse discloses a full-duplex transceiver (see column 5, lines 41 – 46 which would require other ICs to render a functional apparatus).

With regard to claim 6, Phase discloses DSP SERDES wherein at least one of analog serial data and digital data comprises fixed noise pattern (see column 3, lines 35 – 40).

With regard to claim 7, Phanse discloses DSP SERDES wherein DSP determines compensation to be performed to eliminate fixed pattern noise (see column 3, lines 26 – 40).

With regard to claim 8, Phanse discloses DSP SERDES wherein fixed pattern noise is introduced during sampling digital sampling of analog serial data by A/D to generate digital data (see column 3, lines 26 – 40).

With regard to claim 9, Phanse discloses DSP SERDES determines a compensation operation to be performed on analog serial data (see column 4, lines 1 – 21).

With regard to claim 10, Phanse discloses DSP comprises a programmable gain amplifier coupled to A/D converter (see figure 1, 135); and wherein compensation comprises adjusting the gain of programmable gain amplifier (see column 6, lines 59 – 63).

With regard to claim 11, Phanse discloses DSP comprises an AGC controller adjusts AGC gain (see column 6, lines 59 – 63).

With regard to claim 12, Phanse discloses DSP determines a compensation operation to be performed on digital data (see column 11, lines 26 – 38).

With regard to claim 13, Phase discloses DSP is implemented in a data communications application (see abstract).

With regard to claim 14, Phanse discloses DSP further comprising a memory with a plurality of compensation options (see column 12, lines 19 – 25); wherein DSP selects at least one compensation option from plurality of compensation options to ensure proper characteristic of digital data (see column 12, lines 9 – 18).

With regard to claim 15, Phanse discloses DSP wherein proper characteristic of digital data comprises at least one of a gain, a phase, and an offset (see column 11, lines 26 – 38).

With regard to claim 16, Phanse discloses DSP SERDES further comprising a transmitter and an interconnection (see abstract); and wherein interconnection couples transmitter and receiver (see column 3, lines 44 – 53); the transmitter transmits serial data to receiver via interconnection (see column 1, lines 61 – 62); the interconnection comprises a response that introduces an error into serial data (see column 3, lines 4 – 14); the DSP determines error introduced into serial data by response of interconnection (see column 3, lines 26 – 40).

With regard to claim 17, Phanse discloses a proper characteristic of the digital data comprises at least one of a gain, a phase, and an offset; and DSP determines at least one of an error in gain, in phase, or in offset that is introduced during the digital sampling of the incoming serial data by the A/D converter (see column 3, lines 26 – 40).

With regard to claim 18, Phanse discloses DSP compensation comprises adjusting an operational parameter of the A/D converter (see column 6, line 59 – column 7, line 7).

With regard to claim 19, Phanse disclose DSP SERDES further comprising analog circuitry located before and coupled to A/D converter (see figure 1, 125, 130, 135, 140 and abstract).; and wherein compensation determined by DSP comprises compensation operation adjusting parameters of analog circuitry (see figure 1, 160, 165, 170, 175 and abstract).

With regard to claim 20, Phanse discloses DSP SERDES utilizes parallel A/D converters (see column 1, lines 54 – 60 and column 11, lines 52 – 59 where parallel branches are interpreted as having been omitted from drawings); and each A/D converter within plurality performs digital sampling of incoming serial data signal (see column 1, lines 54 – 60 and column 11, lines 52 – 59 where parallel branches are interpreted as having been omitted from drawings).

With regard to claim 21, Phanse discloses DSP SERDES A/D converter within plurality of A/D converters perform digital sampling on the incoming serial data signal (see column 5, line 63 – column 6, line 5) and that Phanse discloses that transfer occurs over 4 pairs of wires which would necessitate 4 circuits (see column 1, lines 54 – 60).

With regard to claim 22, Phanse discloses a DSP SERDES wherein compensation determined by DSP comprises compensation operation that comprises adjusting 1st operational parameter of 1st A/D converter within plurality of A/D converters and 2nd operational parameter of a 2nd A/D converter within the plurality of A/D converters (see

column 6, line 59 – column 7, line 7) and that Phanse discloses that transfer occurs over 4 pairs of wires which would necessitate 4 circuits (see column 1, lines 54 – 60).

With regard to claim 23, Phanse discloses DSP SERDES wherein operational parameters comprises common operational parameters (see column 4, lines 4 – 34) and that Phanse discloses that transfer occurs over 4 pairs of wires which would necessitate 4 circuits (see column 1, lines 54 – 60).

With regard to claim 24, Phanse discloses DSP SERES wherein at least one of operational parameters comprises at least one of gain, phase, and offset (see column 11, lines 26 – 38).

With regard to claim 25, Phanse discloses DSP SERDES wherein A/D converter comprises a plurality of A/D converters; analog serial data is partitioned into a plurality of channels; and each channel of plurality of channels couples to one A/D converter within plurality of A/D converters (see column 1, lines 54 – 60 and column 11, lines 52 – 59 where parallel branches are interpreted as having been omitted from drawings).

With regard to claim 26, Phanse discloses DSP SERDES further comprising a plurality of programmable gain amplifiers(see figure 1, 135); analog serial data is simultaneously fed to each programmable gain amplifier within plurality of programmable gain amplifiers ; outputs of programmable gain amplifiers form the plurality of channels (see column 6, lines 59 – 63; column 1, lines 54 – 60 and column 11, lines 52 – 59 where parallel branches are interpreted as having been omitted from drawings).

With regard to claim 27, Phanse discloses a DSP wherein A/D converter comprises a plurality of A/D converters (see figure 1, 145); analog serial data is simultaneously fed to each A/D converter within plurality of A/D converters (column 1, lines 54 – 60 and column 11, lines 52 – 59 where parallel branches are interpreted as having been omitted from drawings).

With regard to claim 28, Phanse discloses a DSP SERDES further comprising a precursor filter and an equalizer (see figure 1, 140 and column 6, lines 33 – 37) wherein precursor filter and equalizer are coupled to A/D converter.

With regard to claim 29, Phanse discloses DSP SERDES wherein equalizer comprises one of feed forward, feed back, and DFE (see column 10, lines 42 – 55).

With regard to claim 34, Phanse discloses DSP SERDES is operable at Gigabit Ethernet, which operates at a rate of up to 1.25 Gb/s with inclusion of signaling.

With regard to claim 35, Phanse discloses DSP SERDES employs parallel processing compensation techniques (see column 4, lines 1 – 21).

With regard to claim 36, Phanse discloses DSP SERDES comprising at least one additional signal processor that operates cooperatively with DSP (see column 4, lines 4 – 21 where this is interpreted as cooperative arrangement).

With regard to claim 37, Phanse discloses DSP SERDES is operable to perform DSP on digital data to ensure proper characteristics (see column 4, lines 4 – 21).

With regard to claim 38, Phanse discloses DSP SERDES further comprising a crosstalk canceller (see figure 7, 710 and column 11, lines 39 - 59), wherein crosstalk canceller is operable to substantial eliminate at least one of near-end or far-end crosstalk with modulated serial data (see column 11, lines 26 – 37).

With regard to claim 39, Phanse discloses DSP SERDES comprises an analog front end that comprises a plurality of interleaves; and DSP performs adaptive compensation to overcome impairment generated by non-uniformity among interleaves (see abstract).

With regard to claim 40, Phanse discloses DSP SERDES further comprising a plurality of programmable gain amplifiers (see figure 1, 135); analog serial data is simultaneously fed to each programmable gain amplifier within plurality of programmable gain amplifiers; DSP

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performs adaptive compensation to overcome non-uniformity outputs of programmable gain amplifiers form the plurality of channels (see column 6, lines 59 – 63; column 3, lines 26 – 40; column 1, lines 54 – 60 and column 11, lines 52 – 59 where parallel branches are interpreted as having been omitted from drawings).

With regard to claim 41, Phanse discloses a DSP wherein analog front end comprises a plurality of A/D converters (see figure 1, 145); and DSP performs adaptive compensation to overcome impairment generated by non-uniformity among the plurality of A/D converters (see column 3, lines 26 – 40; column 1, lines 54 – 60 and column 11, lines 52 – 59 where parallel branches are interpreted as having been omitted from drawings).

With regard to claim 42, the transceiver claimed is a variation of DSP SERDES of claim 1, and therefore would have been obvious given the aforementioned rejection of claim 1.

With regard to claims 43 – 71 and 76 - 79, these claims are restatements of claims 2 – 29, and 34 - 41 and are similarly analyzed.

With regard to claim 113, the steps claimed as method are a restatement of the functions of the DSP SERDES of claim 1, and therefore would have been obvious given the aforementioned rejection of claim 1.

With regard to claims 114 – 116 and 119 - 128, these claims are restatements of claims 2 – 29 and 34 – 41, and are similarly analyzed.

With regard to claim 134, Phanse teaches these limitations in claim 1 above, plus the additional of limitation of connection via a trace (see column 3, lines 15 – 25 where this is interpreted as inclusive of backplane).

With regard to claims 135 – 162 and 167 - 174, these claims are restatements of claims 2 – 29 and 34 – 41 and are similarly analyzed.

With regard to claim 179, transceiver claimed is a variation of DSP SERDES of claim 1, and therefore would have been obvious given the aforementioned rejection of claim 1.

With regard to claim 180, Phanse teaches these limitations in claim 179 above, plus the additional of limitation of connection via a trace (see column 3, lines 15 – 25 where this is interpreted as inclusive of backplane).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 30 – 33, 72 – 75, 80 – 112, 117, 118, and 163 – 166 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phanse ('494) in view of Jamali (US-6,678,319).

With regard to claim 30, Phanse is silent with respect to decoder, however he does disclose that signals are encoded (see column 2, lines 5 – 7). Jamali discloses DSP SERDES comprising a decoder to decode digital samples of modulated data (see figure 3, 328). It would have been obvious to one of ordinary skill in the art at the time of invention to include decoder in system as it is an integral part of the Gigabit Ethernet standard.

With regard to claim 31, Phanse discloses use of parity check or trellis coding (see column 2, lines 5 – 7).

With regard to claim 32, Phanse is silent with respect to Viterbi decoder. Jamali discloses DSP SERDES comprising a Viterbi decoder to decode ISI within the modulated

data (see figure 3, 328 and column 2, lines 44 - 46). It would have been obvious to one of ordinary skill in the art at the time of invention to include decoder in the system as it is an integral part of the Gigabit Ethernet standard.

With regard to claim 33, Phanse is silent with respect to Viterbi decoder. Jamali discloses DSP SERDES comprising a Viterbi decoder (see figure 3, 328 and column 2, lines 44 - 46), but is silent with regard to algorithm implemented. It would have been obvious to one of ordinary skill in the art at the time of invention to include Viterbi decoder using some form of maximum likelihood detection as it is one of a known form of detection algorithms.

With regard to claims 72 - 75, these claims are restatements of claims 30 - 33 and are similarly analyzed.

With regard to claim 80, Phanse discloses the limitations of a transceiver as analyzed in claim 1 but is silent with respect to feedback equalizer. Jamali discloses a transceiver utilizing a feedback equalizer (see figure 5, 528) for adjustment of channel characteristics (see column 5, lines 19 - 51). It would have been obvious to one of ordinary skill in the art at the time of invention to utilize a feedback equalizer to improve system performance (see '319, column 3, lines 48 - 51).

With regard to claims 81 - 104 and 109 - 112, these claims are restatements of claims 2 - 29 and 34 - 41, and are similarly analyzed.

With regard to claims 105 - 108, these claims are restatements of claims 30 - 33, and are similarly analyzed.

With regard to claims 117 and 118, these claims are restatements of claims 30 - 33, and are similarly analyzed.

With regard to claims 163 - 166, these claims are restatements of claims 30 - 33, and are similarly analyzed.

4. Claims 129 – 133, 175 – 178, and 181 - 184 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phanse ('494) in view of Apple (US-5,239,299).

With regard to claim 129, the steps claimed as method are a restatement of the function of the DSP SERDES of clam 1 with the additional limitation of pre-computing possible compensation operations (see column 4, lines 5 – 21 where this is interpreted as equivalent). Phanse is silent with respect to sequential sampling of interleaved A/D converters. Apple discloses sequentially sampled, interleaved A/D converters with digital compensation. It would have been obvious to one of ordinary skill in the art at the time of invention to utilize multiple A/D converters to improve sampling speed ('299, column 1, lines 20 – 30), and thus channel bandwidth.

With regard to claims 130 – 133, these claims are restatements of claims 2 – 41 and are similarly analyzed.

With regard to claim 175, Phanse discloses a DSP SERDES as described in claim 1. Phanse is silent with respect to plurality of interleaved A/D converters. Apple discloses sequentially sampled, interleaved A/D converters with digital compensation. It would have been obvious to one of ordinary skill in the art at the time of invention to utilize multiple A/D converters to improve sampling speed ('299, column 1, lines 20 – 30), and thus channel bandwidth.

With regard to claim 176, Phanse / Apple discloses the limitations of claim 175 above. Phanse is silent with respect to compensation of non-uniformity of interleaved A/D converters. Apple discloses means for the compensation of non-uniformity between interleaved A/D converters (see abstract). It would have been obvious to one of ordinary skill in the art at the

time of invention to utilize equalization techniques to produce a higher quality conversion process (see column 1, lines 43 – 50).

With regard to claim 177, Phanse / Apple teaches these limitations in claim 176 above, plus the additional of limitation of connection via a trace (see column 3, lines 15 – 25 where this is interpreted as inclusive of backplane).

With regard to claim 178, Phanse / Apple teaches these limitations in claim 175 above, plus the additional of limitation of connection via a trace (see column 3, lines 15 – 25 where this is interpreted as inclusive of backplane).

With regard to claim 181, Phanse discloses a DSP SERDES as described in claim 1 with additional limitation of parallel processing of data (see column 1, line 61 – column 2, line 8 where this is interpreted as parallel processing of data streams). Phanse is silent with respect to plurality of interleaved A/D converters. Apple discloses sequentially sampled, interleaved A/D converters with digital compensation. It would have been obvious to one of ordinary skill in the art at the time of invention to utilize multiple A/D converters to improve sampling speed ('299, column 1, lines 20 – 30), and thus channel bandwidth.

With regard to claim 182, Phanse / Apple teaches these limitations in claim 181 above, plus the additional of limitation of connection via a trace (see column 3, lines 15 – 25 where this is interpreted as inclusive of backplane).

With regard to 183, this claim is similarly analyzed to claim 177 above.

With regard to claim 184, Phanse / Apple teaches these limitations in claim 183 above, plus the additional of limitation of connection via a trace (see column 3, lines 15 – 25 where this is interpreted as inclusive of backplane).

Other Cited Prior Art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Miki (US-4,968,988), Corcoran (US-5,294,926), and Kost (US-6,081,215) all disclose apparatus and methods relating to usage of interleaved A/D conversion. Corcoran and Kost further disclose compensation techniques for A/D conversion non-uniformities.

Nobakht (US-6,009,120) discloses an equalizer suitable for use in Gigabit Ethernet applications.

Azadet (US-6,363,112) discloses a parallel processing DFE suitable for use in Gigabit Ethernet applications.

Trans (US-6,377,640) discloses a communication system suitable for use in Gigabit Ethernet applications comprising many features of applicant's claimed invention.

Raghavan (US-6,438,163) discloses an equalizer and method suitable for Gigabit Ethernet applications.

Daball (US-6,621,862) discloses a method and apparatus for use in data communication networks with many similar features and functions to applicant's claimed invention.

Fiedler (US-6,731,683) discloses an equalizer suitable for use in serial data stream applications.

Koyama (US-6,859,508) discloses a multi-dimensional equalizer and FEXT canceller suitable for use in Gigabit Ethernet applications.

Kim (US-6,934,387) discloses a NEXT and FEXT canceller with adaptive correlation suitable for use in Gigabit Ethernet applications.

NPL references are furnished to show a general state of knowledge in the art regarding claimed invention.

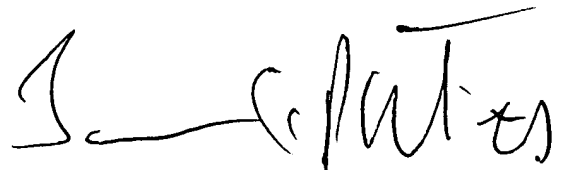
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Meek whose telephone number is (571)272-3013. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571)272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMM
9/30/05



**JAY K. PATEL
SUPERVISORY PATENT EXAMINER**